REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-16 are pending in this application. Claim 1 was rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 6,667,214 to Yamada. Claims 2-16 were objected to as dependent upon a rejected base claim, but were noted as allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

Initially, applicants gratefully acknowledge the indication of the allowable subject matter in claims 2-16.

Addressing now the rejection of claim 1 under 35 U.S.C. § 102(e) as anticipated by Yamada, that rejection is traversed by the present response.

Applicants respectfully submit independent claim 1 positively recites features neither taught nor suggested by Yamada.

First, independent claim 1 positively recites "a device substrate having a semiconductor layer separated by a dielectric layer from a base substrate". That feature is believed to clearly distinguish over the teachings in Yamada.

With respect to the above-noted feature the outstanding Office Action cites Figure 3 of Yamada disclosing a semiconductor layer 25 separated by a dielectric layer 11 from a base substrate 10. However, applicants respectfully submit those elements noted in Yamada do not correspond to the claimed features.

In Figure 3 Yamada discloses a semiconductor memory device including memory cells formed on layer 11, which is formed on a substrate 10. Applicants note element 11 in Yamada is a well and is not in fact a dielectric layer. Applicants also note no disclosure has been cited in Yamada to disclose that well 11 is a dielectric layer. Applicants respectfully submit the well 11 in Yamada is apparently made of a semiconductor, and there is no disclosure in Yamada for construing that the well 11 is made of a dielectric material.

Applicants also note the impurity diffusion layer 25 in Yamada is a small layer formed just below the gate dielectric layer 20, and in that respect applicants submit the small impurity diffusion layer 25 is not a "device substrate".

Independent claim 1 also additionally recites "a memory cell array ... including diffusion layers formed on said device substrate and a body between the diffusion layers, said body being in an electrically floating state to store data based on a majority carrier accumulation state of said body". That positively claimed structure is also not met by Yamada.

In the rejection applicants note elements 14 and 16 appear to be cited with respect to the claimed diffusion layers. However, as is clear from Figure 3 in Yamada those elements 14 and 16 are not are not formed on the layer 25, which is noted as corresponding to the device substrate. Claim 1 requires "diffusion layers ***formed on*** said device substrate". Clearly in Yamada diffusion layers 14 and 16 are ***not formed on*** the layer 25.

Further, applicants note that in contrast to the claimed features Yamada discloses a so-called stacked gate transistor memory cell. In that structure data is stored by injecting hot electrons into the floating gate 22,[1] which is a different method than in the present invention.

The outstanding rejection also appears to cite the diffusion layer 25 as corresponding to the "body being in an electrically floating state to store data". In that respect applicants request clarification of the rejection as layer 25 in Yamada was also cited as corresponding to the claimed "semiconductor layer" of the device substrate. Clearly that layer 25 in Yamada does not meet the limitation of both the claimed "semiconductor layer" and a "body between the diffusion layer".

Applicants also note that as well 11 in Yamada is not a dielectric layer, as discussed above, the layer 25 cannot be in "an electrically floating state". Applicants also note that the

[1] See Yamada at column 12, lines 45-55.

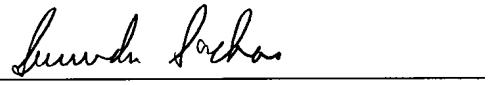
layer 25 is not constructed to "store data". In claim 1 the body which is in an electrically floating state is configured to "store data", which again clearly differs from the teachings of layer 25 in Yamada.

In such ways, applicants respectfully submit independent claim 1 clearly distinguishes over the teachings in Yamada.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Registration No. 28,870
Surinder Sachar
Registration No. 34,423
Attorneys of Record

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

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